DIGITAL LOGIC LAB KL-300

The KL-300 Digital Logic Lab is a comprehensive and self-contained system suitable for anyone engaged in digital logic experiments. All necessary equipments for digital logic experiments such as power supply, signal generator, switches and displays are installed on the main unit. The 13 modules covers a wide variety of essential topics in the field of digital logic. It is a time and cost saving device for both students and researchers interested in developing and testing circuit prototypes.

- *Suitable for combined logic, sequential logic and microprocessor circuits designing and experiments.*
- *Ideal tool for learning the basics of digital logic circuits.*
- *Comprehensive power, signal supply and testing devices for convenient experiments.*
- *Expandability and flexibility of experiments greatly increased with universal breadboard.*
- *Capable of processing TTL, CMOS, NMOS, PMOS and ELC circuits.*
- *All supply units are equipped with overload protection for better safety.*
- *All modules equipped with 8-bit DIP switch for fault simulations.*

- *Individual storage cases for all modules for easy storing and carrying.*

SPECIFICATION

MAIN UNIT (KL-31001)

POWER SUPPLY

① **Dual DC Power Supply**
(1) Voltage Range: +5V, 1.5A; -5V, 0.3A; ±12V, 0.3A
(2) With overload protection.

② **Adjustable DC Power Supply**
(1) Voltage Range : +1.5V~+15V
(2) Maximum Current Output : 0.5A
(3) With overload protection.

SIGNAL GENERATOR

All signal generators has independent and simultaneous TTL and CMOS level output terminal. CMOS level output range from +1.5V to +15V and is controlled from the voltage adjustment knob of the Adjustable DC Power Supply.

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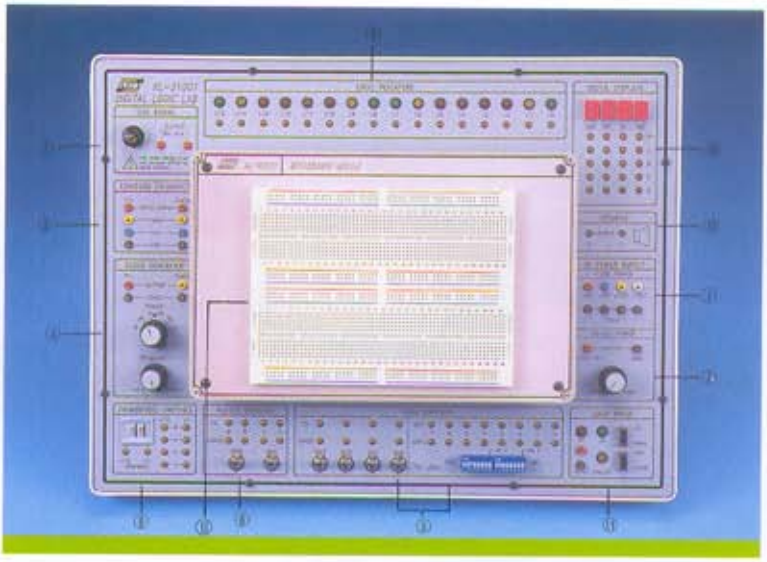
KL-300 DIGITAL LOGIC LAB



③ **Standard Frequency**
(1) Frequency : 1MHz, 60Hz, 1Hz
(2) Accuracy : ±0.01% (1MHz)
(3) Fanout : 10 TTL load

④ **Clock Signal Generator**
(1) Frequency : 1Hz ~ 1MHz (6 Ranges)
a. 1Hz ~ 10Hz d. 1KHz ~ 10KHz
b. 10Hz ~ 100Hz e. 10KHz ~ 100KHz
c. 100Hz ~ 1KHz f. 100KHz ~ 1MHz
(2) Fanout: 10 TTL load

⑤ **Data Switch**
(1) 2 × 8-bit DIP switch, 16-bit TTL level output.
(2) 4 × toggle switch, each with DEBOUNCE circuit
(3) Fanout : 10 TTL load

⑥ **Pulser Switch**
(1) 2 sets of independent control output.
(2) Each set with Q, Q output, pulse width > 5mS
(3) Each set of switch with DEBOUNCE circuit
(4) Fanout : 10 TTL load

⑦ **Line Signal Generator**
(1) Frequency : 60Hz (3) With overload protection.
(2) Output Voltage : 6Vrms

⑧ **Thumbwheel Switch**
2-digit, BCD code output, common point input

DISPLAY

⑨ **Logic Indicator**
(1) 16 sets of independent LED indicates high and low logic state.
(2) Input Impedence: < 100KΩ

⑩ **Digital Display**
(1) 4 sets of independent 7-segment LED display.
(2) With BCD, 7-segment decorder/driver and Dp input terminal.
(3) Input with 8-4-2-1 code.

TESTING DEVICES

⑪ **Logic Probe**
(1) TTL and CMOS level.
(2) 3mm LED displays.
(3) "Lo" and "Hi" LED displays low and high logic state respectively.

⑫ **Speaker**
An 8Ω, 0.25W speaker with driver circuit.

BREADBOARD MOUDLE

⑬ **Breadboard**
1680 tie-point breadboard on top panel can be easily put into and taken off.

ACCESSORIES

⑭ **A. Connect Leads: (1) 2mm-0.65mm, 300mmL, 6pcs**
(2) 2mm-2mm, 450mmL, 10pcs
B. Test Probe: 2mm-2mm, 600mmL, 1pc
C. User's Manual
D. Fuse
E. AC Cord
F. Anti-Dust Cover

EXPERIMENT MODULES

1. All 13 modules equipped with an 8-bit DIP switch for fault simulation. Users learn how to solve various problems by setting the DIP switch to different positions.
2. Solutions for all faults are listed in the experiment manual for user's reference.
3. 2mm plugs and sockets used throughout the lab and all modules.
4. Comprehensive experiment and instructor's manual.
5. Module dimension: 265 × 165 × 30mm.
6. Connection plugs are used on the modules to prevent accidental damages.
7. Individual storage case for each module.

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MODULES AND THE EXPERIMENTS THEY PERFORM


KL-33001 Basic Logic Gates Experiments


KL-33002 Assembled Logic Circuit Experiments (1)


KL-33003 Assembled Logic Circuit Experiments (2)


KL-33004 Assembled Logic Circuit Experiments (3)


KL-33005 Assembled Logic Circuit Experiments (4)


KL-33006 Assembled Logic Circuit Experiments (5)


KL-33007 Clock Generator Circuit Experiments


KL-33008 Sequential Logic Circuit Experiments (1)


KL-33009 Sequential Logic Circuit Experiments (2)


KL-33010 Memory Circuit Experiments (1)


KL-33011 Memory Circuit Experiments (2)


KL-33012 Converter Circuit Experiments (1)


KL-33013 Converter Circuit Experiments (2)

LIST OF EXPERIMENTS

1. Basic Logic Gates Experiments

1-1 Introduction to Logics and Switches ..... KL-33001(A)
1-2 Logic Gates Circuits
- a. Diode Logic (DL) Circuit ..... KL-33001(C)
- b. Resistor-Transistor Logic (RTL) Circuit ..... KL-33001(B)
- c. Diode-Transistor Logic (DTL) Circuit ..... KL-33001(B,C)
- d. Transistor-Transistor Logic (TTL) Circuit ..... KL-33001(D)
- e. CMOS Logic Circuit ..... KL-33001(E)

1-3 Threshold Voltage Measurement
- a. TTL Threshold Voltage Measurement ..... KL-33001(A)
- b. CMOS Threshold Voltage Measurement ..... KL-33001(B)

1-4 Voltage/Current Measurement
- a. TTL I/O Voltage/Current Measurement ..... KL-33001(A)
- b. CMOS Voltage/Current Measurement ..... KL-33001(B)

1-5 Basic Logic Gate Transmission Delay Measurement
- a. TTL Gate Delay Time Measurement ..... KL-33001(A)
- b. CMOS Gate Delay Time Measurement ..... KL-33001(A)

1-6 Measurement of Basic Logic Gates Characteristics
- a. AND Gate Characteristics Measurement ..... KL-33001(A,B)
- b. OR Gate Characteristics Measurement ..... KL-33001(A,B)
- c. INVERTER Gate Characteristics Measurement ..... KL-33001(A,B)
- d. NAND Gate Characteristics Measurement ..... KL-33001(A,B)
- e. NOR Gate Characteristics Measurement ..... KL-33001(A,B)
- f. XOR Gate Characteristics Measurement ..... KL-33001(A,B)

1-7 Interface Between Logic Gates
- a. TTL to CMOS interface ..... KL-33001(A)
- b. CMOS to TTL interface ..... KL-33001(B)

2. Combinational Logic Circuits Experiments

2-1 NOR Gate Circuit ..... KL-33002(A)
2-2 NAND Gate Circuit ..... KL-33002(B)
2-3 XOR Gate Circuit
- a. Constructing XOR Gate with NAND Gate ..... KL-33002(B)
- b. Constructing XOR Gate with Basic Gate ..... KL-33002(C)

2-4 AND-OR-INVERT (AOI) Gate Circuit ..... KL-33002(C)
2-5 Comparator Circuits
- a. Comparator Constructed with Basic Logic Gates ..... KL-33002(C)
- b. Comparator Constructed with TTL IC ..... KL-33002(D)

2-6 Schmitt Gate Circuit ..... KL-33002(A)
2-7 Open-Collector Gate Circuits
- a. High Voltage/Current Circuit ..... KL-33002(E)
- b. Constructing an AND Gate with Open-Collector Gate ..... KL-33002(E)

2-8 Tristate Gate Circuits
- a. Truth Table Measurements ..... KL-33003(C)
- b. Constructig an AND Gate with Tristate Gate ..... KL-33003(C)
- c. Bidirectional Transmission Circuit ..... KL-33003(C)

2-9 Half-Adder and Full-Adder Circuits
- a. Constructing HA with Basic Logic Gates ..... KL-33004(A)
- b. Full Adder Circuit with IC ..... KL-33004(B)
- c. High-Speed Adder Carry Generator Circuit ..... KL-33003(A)
- d. BCD Code Adder Circuit ..... KL-33004(B)

2-10 Half-Subtractor and Full-Subtractor Circuit
- a. Subtractor Circuit Constructed with Basic Logic Gates ..... KL-33004(A)
- b. Full Adder and Inverter Circuit ..... KL-33004(B)

2-11 Arithmetic Logic Unit (ALU) Circuit ..... KL-33003(B)
2-12 Bit Parity Generator Circuit
- a. Bit Parity Generator Constructed with XOR Gates ..... KL-33004(A)
- b. Bit Parity Generator IC ..... KL-33003(C)

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2-13 Encoder Circuit
- a. Constructing a 4-to-2 Encoder with Basic Gates ..... KL-33005(A)
- b. Constructing a 10-to-4 Encoder with TTL IC ..... KL-33004(C)

2-14 Decoder Circuit
- a. Constructing a 2-to-4 Decoder with Basic Gates ..... KL-33005(C)
- b. Constructing a 4-to-10 Decoder with TTL IC ..... KL-33004(C)

2-15 Multiplexer Circuit
- a. Constructing a 2-to-1 Multiplexer ..... KL-33006(E)
- b. Using Multiplexers to Create Functions ..... KL-33006(F)
- c. Constructing a 8-to-1 Multiplexer with TTL IC ..... KL-33006(F)

2-16 Demultiplexer Circuit
- a. Constructing a 2-output Demultiplexer ..... KL-33006(E)
- b. Constructing a 8-output Demultiplexer ..... KL-33006(B)

2-17 Digitally Controlled Analog Multiplexer/Demultiplexer Circuit
- a. Analog Switch Characteristics ..... KL-33006(C,D)
- b. Bidirectional Transmission with CMOS IC Analog Switches ..... KL-33006(C)

3. Clock Generator Circuit Experiments

3-1 Constructing Oscillator Circuit with Basic Logic Gates ..... KL-33007(A)
3-2 Constructing Oscillator Circuit with Schmitt Gate ..... KL-33007(B)
3-3 Voltage Controlled Oscillator (VCO) Circuit ..... KL-33007(C)
3-4 555 IC Oscillator Circuit
- a. 555 Oscillator Circuit ..... KL-33007(D)
- b. VCO Circuit ..... KL-33007(D)

3-5 Monstable Multivibrator Circuits
- a. Low-Speed Monostable Multivibrator Circuits ..... KL-33007(E)
- b. High-Speed Monostable Multivibrator Circuits ..... KL-33007(E)
- c. Constructing Monostable Multivibrator Circuits ..... KL-33007(D)
- d. Constructing Non-Retriggerable Circuit with TTL-IC ..... KL-33007(F)
- e. Constructing Retriggerable Circuit with TTL-IC ..... KL-33007(G)
- f. Constructing a Variable Duty Cycle Oscillator Circuit with Monostable Multivibrator ..... KL-33008(A)

4. Sequential Logic Circuit Experiments

4-1 Flip-Flop Circuits
- a. Constructing a R-S Flip-Flop with a Basic Logic Gates ..... KL-33008(D)
- b. Constructing a D Flip-Flop with a R-S Flip-Flop ..... KL-33008(D)
- c. Constructing a T Flip-Flop with a D Flip-Flop ..... KL-33008(D)
- d. Constructing a J-K Flip-Flop with a R-S Flip-Flop ..... KL-33008(D)
- e. Constructing a Shift Register with a D Flip-Flop ..... KL-33008(C)
- f. Preset Left/Right Shift Register ..... KL-33008(B)
- g. Constructing A Noise Elimination Circuit with R-S Flip-Flop ..... KL-33008(D)

4-2 J-K Flip-Flop Circuits
- a. Asynchronous Binary Up-Counter ..... KL-33009(A)
- b. Asynchronous Decade Up-Counter ..... KL-33010(D)
- c. Asynchronous Divide-by-N Up-Counter ..... KL-33010(C)
- d. Asynchronous Binary Down-Counter ..... KL-33009(A)
- e. Synchronous Binary Up-Counter ..... KL-33009(A)
- f. Synchronous Binary Up/Down Counter ..... KL-33009(A)
- g. Presetable Synchronous Binary Up/Down Counter ..... KL-33010(A)
- h. Presetable Synchronous Decimal Up/Down Counter ..... KL-33010(B)
- i. Ring Counter ..... KL-33009(A)
- j. Johnson's Counter ..... KL-33009(A)

5. Memory Circuit Experiments

5-1 Constructing READ ONLY MEMORY (ROM) with Diodes ..... KL-33010(F)
5-2 Constructing RANDOM ACCESS MEMORY (RAM) with D Flip-Flop ..... KL-33010(G)
5-3 64-bit RAM Circuit ..... KL-33011(B)
5-4 ERASABLR PROGRAMMABLE READ ONLY MEMORY (EPROM) Circuit ..... KL-33010(E)
5-5 Electronic EPROM (EEPROM) Circuit ..... KL-33011(A)
5-6 Constructing Dynamic Scanning Counter with Single-chip Microprocessor ..... KL-33012(A)

6. Converter Circuit Experiment

6-1 Digital/Analog Converter (DAC) Circuit
- a. Unipolar DAC Circuit ..... KL-33013(A)
- b. Bipolar DAC Circuit ..... KL-33013(A)

6-2 Analog/Digital Converter (ADC) Circuit
- a. 8-bit Converter Circuit ..... KL-33012(B)
- b. 3 1/2-digit Converter Circuit ..... KL-33013(B)

ACCESSORIES (KL-38002)

A. Connect Leads: 2mm-2mm, 300mmL, 25pcs
B. Connect Plugs: ø2mm, 10mmL, 15pcs
C. Experiment manual and Instructor's manual.
D. Key: 1pc

GENERAL CHARACTERISTICS

A. Individual storage case for each module (205×295×65mm).
B. Power Source : 110V/220V±10%, 50/60Hz
C. Operating Temperature: 0°c~50°c
D. Humidity : <90% relative humidity
E. Dimension : 400×300×130mm
F. Weight : Approx. 5. Kg